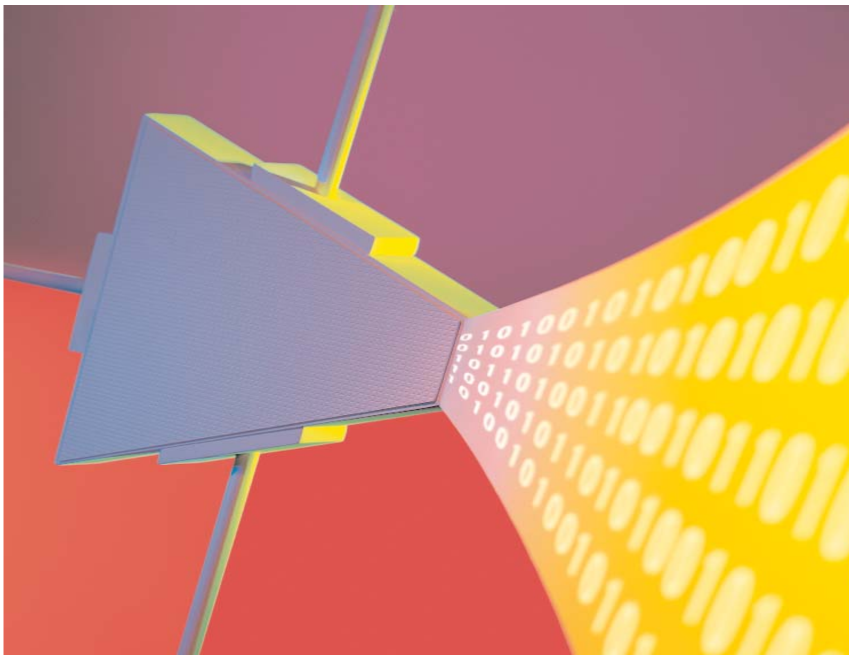
TESTKOMPRESS

ATPG WITH EMBEDDED COMPRESSION

Design-for-Test

D A T A S H E E T



Mentor Graphics TestKompress enables semiconductor manufacturers to improve test quality while reducing test costs.

IMPROVE TEST QUALITY WHILE REDUCING OVERALL TEST COST

As process technologies migrate to sub-100 nanometer, high quality test is a key factor for maintaining low defect rates. The TestKompress® product uses patented Embedded Deterministic Test (EDT™) technology to dramatically reduce the amount of test data required for today's complex integrated circuits (ICs) while maintaining test quality. With up to a 100X reduction in test data volume and test time, compared to state-of-the-art scan and automatic test pattern generation (ATPG) methodologies, semiconductor manufacturers can dramatically increase the quantity and quality of tests they perform while controlling costs.

Using advanced deterministic pattern generation, TestKompress ensures high test coverage. For improved test quality, TestKompress supports at-speed transition and path delay pattern generation using either a launch-off-shift or launch-off-capture application methodology.

Using TestKompress, semiconductor manufacturers can attain higher product quality with less stored test data and shorter test times. This increases production throughput, eliminates the need for tester memory upgrades, enables the use of less expensive structural testers, and extends the life of existing automatic test equipment.

EMBEDDED DETERMINISTIC TEST TECHNOLOGY

The EDT technology builds on the solid foundation of scan and ATPG. EDT consists of logic embedded on-chip and a new deterministic pattern generation technique.

The EDT logic is inserted in the scan path outside of the design core and consists of two main blocks: a decompressor, which feeds a large number of internal scan chains from a small number of scan channels; and, a selective compactor, which compacts the response to the scan channel outputs. Using EDT, designers can insert

HIGH TEST QUALITY

- High test coverage ensured by deterministic pattern generation
- 100X compression of scan test time and data, enabling testing of additional fault types and eliminating the need for pattern truncation
- Comprehensive set of fault models, such as stuck-at, IDDQ, bridging, transition, and path-delay for at-speed test and ability to support any future fault models needed
- Same pattern types as FastScan ATPG for maximum coverage, including basic, clock-sequential, RAM-sequential, clock PO, and multi-load

TEST COST REDUCTION

- Increased production throughput; scan test time reduced up to 100X
- Less tester memory required; scan test volume reduced up to 100X

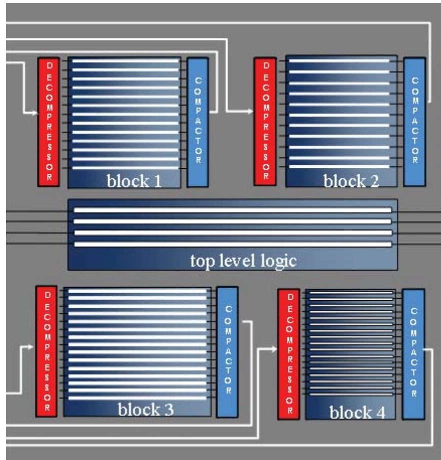
NO DESIGN IMPACT

- No system logic modifications; compression logic is located outside the functional logic
- No performance impact; no need to test points or X-bounding logic
- Design style independence, supports all design sizes and types; no special handling for embedded blocks, memories, or non-scan cells required

SCAN/ATPG DESIGN FLOW

- Easy to use, based on scan and ATPG; utilizes the FastScan™ command set. Fully compatible with Mentor's entire suite of DFT products
- Design flow independent, fits easily into any scan-based design flow, hierarchical or block-based

designers can insert 100X or more, and therefore 100X shorter, internal scan chains than traditional scan while still utilizing the same number of external tester scan channels and package scan pins. EDT is unique in that it can even support the use of only one scan in and one scan out channel.



Interface and top-level logic are automatically tested; no top level logic required. Blocks need as few as one scan in and out for top level routing.

The embedded decompressor and compactor are located only in the scan path, so critical timing closure issues are not impacted and no changes to the core design are needed. The TestKompress tool handles unknown states that could result in fault masking as well as fault aliasing. No additional logic, such as test points or X-bounding, is required.

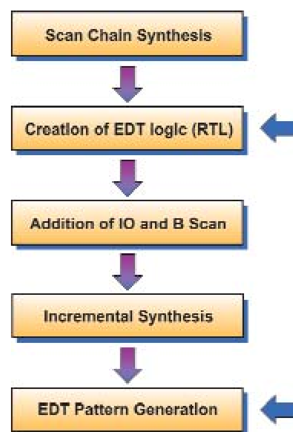
IMPROVING YIELD

Rapid failure diagnosis is key to quickly ramping up production yields, and hence, profitability. TestKompress aids failure analysis by directly analyzing the compressed failing test responses to determine the probable defect sites within a device. This method eliminates the need for retesting a failing device in a special diagnostics mode, or with special diagnostics patterns, and expedites a process that can take weeks to perform manually.

DESIGN FLOW AND INTEGRATION

TestKompress fits into any scan-based design flow and uses the same commands and design rule checks (DRCs) as FastScan. Because of the similarity to traditional scan/ATPG flows, users of FastScan and other ATPG tools can easily adopt an EDT methodology.

TestKompress can even add compression logic independently for each module in a design. This allows design teams working on individual modules to incorporate all the test logic and to verify all the test logic as each block is being designed. At the top-level, pattern generation is capable of controlling each decompressor and compactor at the same time to create an optimized test.



A design flow with TestKompress is similar to a flow with traditional scan and ATPG. TestKompress is used to create both the EDT logic and generate compressed patterns.

TestKompress is part of the Mentor Graphics suite of technology-leading DFT tools, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit www.mentor.com/dft.

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Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503-685-7000

Sales and Product Information
Phone: 800-547-3000
503-685-8000

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, CA 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303

Mentor Graphics Europe
Mentor Graphics Corporation
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140-0001
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3021

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