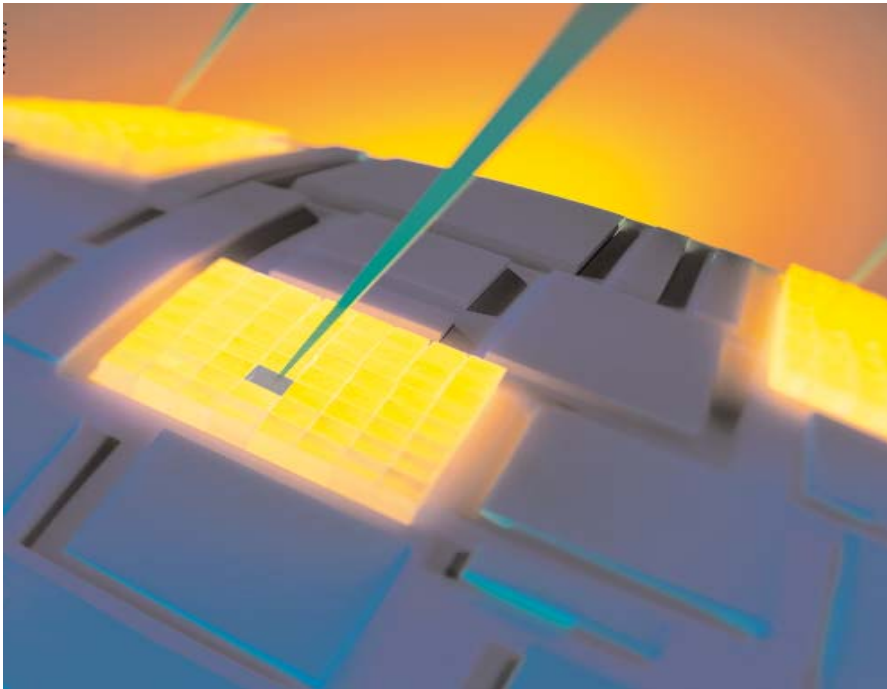


MBISTARCHITECT

AUTOMATED MEMORY BUILT-IN SELF-TEST

Design-for-Test

D A T A S H E E T



MBISTArchitect provides complete automation of memory BIST.

TESTING EMBEDDED MEMORIES

Embedded memory continues to represent a larger portion of today's challenging designs. Because of this trend, and the nature of a memory's small geometries, implementing a sound memory testing strategy is one of the most significant design decisions.

Mentor Graphics MBISTArchitect™ tool provides all of the features required for testing embedded memories by applying built-in self-test (BIST). The tool is used to generate complete register transfer level (RTL) test logic that can be applied to an unlimited number of memories, with varying sizes and configurations. The tool also integrates the MBIST controllers into the design at the RTL or gate level, and generates the chip level testbench and patterns for ATE.

The rich feature set of MBISTArchitect efficiently addresses three key areas to ensure all embedded SRAMs and ROMs are thoroughly tested: high test quality, easy application, and versatility.

HIGH TEST QUALITY

The fine geometries typical of an embedded memory make it susceptible to subtle defects. This requires a thorough set of test patterns strategically chosen to expose manufacturing defects. MBISTArchitect creates test circuitry that applies, reads, and compares pattern algorithms to detect these defects. It allows users to choose from the largest set of industry-standard memory test algorithms. These algorithms include the common "March" and checkerboard algorithms, varied pattern backgrounds, and many others. For memories requiring the application of proprietary algorithms, MBISTArchitect offers the user-definable algorithm features.

Many faults are only observable when memories are run at their maximum operating speed. MBISTArchitect applies patterns at-speed to ensure higher coverage of speed-related defects. In fact, the MBIST Full-Speed™ feature can accelerate at-speed test by up to a factor of three.

HIGH QUALITY EFFICIENT TEST

- Supports the largest set of algorithms for flexible, high-quality memory test
- Delivers the fastest at-speed testing for efficient, high-quality test
- Enables customized algorithms for maximum flexibility and test coverage
- Supports all algorithms for recommended for Artisan memory test

DIAGNOSTICS & REPAIR

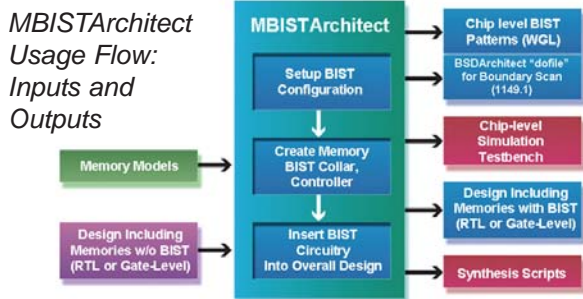
- Offers comprehensive diagnostics for failure analysis
- Supports memory repair for yield improvement
- Supports diagnosis for at-speed test

DESIGN FLOW

- Creates a simulation testbench for verification and WGL format patterns for ATE
- Libraries endorsed and supported by leading memory vendors for ease of adoption
- Online algorithm selection
- Top-down, block-based and bottom-up MBIST logic insertion flows
- Data-slicing for reduced routing between MBIST controller and memories



Using a patented, pipe-lining technique, MBIST Full-Speed simultaneously applies patterns, reads them back, and compares the results. This process produces the highest quality test in the shortest amount of time.



EASY APPLICATION

Memory test concerns should not consume valuable design time. MBISTArchitect automates the entire process by simply reading a model of the memory and creating the entire BIST circuitry in RTL. Memories can be tested concurrently or sequentially, and users can determine which memories share controllers.

With the memory test management feature, the entire set of memory BIST circuits can be inserted into an overall design, allowing control of which memories share controllers and the sequence for testing in a single pass flow. To quickly verify BIST insertion, MBISTArchitect automatically creates a simulation testbench. MBIST controller integration into the design can be handled at the RTL or gate level, and the tool also creates the WGL format patterns at the chip level for use with ATEs.

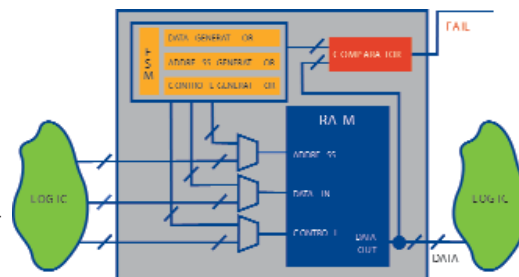
One of the tool's most important features is award-winning customer support. Mentor Graphics employs an expert staff of support engineers who specialize in design-for-test (DFT) and can assist in the memory BIST process if necessary.

VERSATILITY

The rapidly changing world of memory technology requires a tool that can adapt to many different technologies and test configurations. MBISTArchitect supports a wide variety of memory

configurations, including those with multiple ports, data scrambling, and pre-configured BIST access. MBISTArchitect is used by a broad range of customers, from large semiconductor companies to small fabless operations, and Mentor Graphics works closely with these customers to develop ongoing tool enhancements that keep pace with changing technology and needs. This development process insures users have access to the latest and most comprehensive memory testing technology available.

When faults are identified within a memory, on-chip diagnostics can be used to pinpoint the exact location of fault. This information is sent out in a serial fashion, typically through boundary scan.



MBISTArchitect automates the creation of BIST circuitry for comprehensive testing of embedded memories.

For users of BSDArchitect™, Mentor's 1149.1-2001 compliant boundary scan tool, this interface is automated. MBISTArchitect also utilizes redundant memory columns and rows for memory "repair." The BIST process automatically determines the defective columns and rows and outputs its location, eliminating the need for off-chip calculations.

MBISTArchitect is supported by many of the leading memory vendors including ARM, Mosys and Dolphin. These companies provide the model libraries needed to get users up and running.

MBISTArchitect is part of the Mentor Graphics technology-leading DFT tool suite, which includes integrated solutions for scan, ATPG, Test time/data compression, advanced memory test, logic BIST, boundary scan, diagnosis, and a variety of DFT-related flows. All Mentor DFT tools are available on UNIX and Linux platforms. For more information, visit www.mentor.com/dft.

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