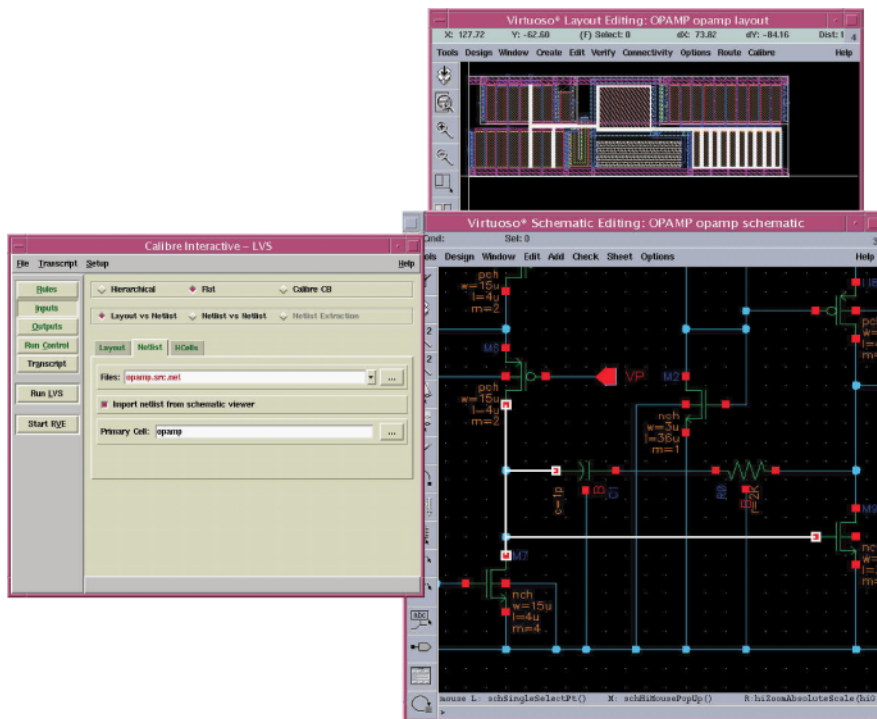


Calibre LVS



Calibre LVS, shown here invoked from within the Cadence® Virtuoso layout environment through Calibre Interactive, offers efficient and accurate layout device and connectivity extraction as well as circuit comparison with the schematic.

Calibre LVS: Precise IC Layout Verification with the Schematic Design

Calibre® LVS, the market-leading layout vs. schematic physical verification tool, is tightly linked with both Calibre DRC and Calibre xRC to deliver production-proven device extraction for both physical verification and parasitic extraction. Calibre LVS performs a vital function as a member of a complete IC verification tool suite by providing device and connectivity comparisons between the IC layout and the schematic. Calibre's hierarchical processing engine runs Calibre LVS in tandem with Calibre DRC and Calibre xRC, supplying data for modifying the IC design to achieve superior functionality and reliability. Calibre LVS is unique among LVS tools because it measures actual device geometries for a complete accounting of physical parameters. These precise device parameters supply the information for back-annotation to the source schematic and the comprehensive data for running simulations.

Calibre's ability to interactively verify and make corrections in an existing design framework, without being constrained by proprietary tools or flows, dramatically reduces iteration runtime and error debugging. This robust and easy-to-use integration enables designers to use Calibre as a single platform for cell/block and full-chip verification, as well as parasitic extraction.

Key Product Benefits

- **Precise Design Back Annotation.** Extracts accurate device layout, connectivity and circuit comparison data for verification with the schematic layout.
- **Complete Device Parameter Analysis.** Verifies that the physical layout is equivalent to the device model by extracting and measuring the actual physical geometries in the layout.
- **Short Isolation Capabilities.** Identifies and isolates the shortest paths between mismatched text labels on the same electrical net.
- **Flexible Parameter Calculations with Built-In Functions.** Calculates default property values automatically, such as transistor length and width, and built-in functions allow the user to perform custom parameter calculations.
- **Stress Effects Management.** Measures physical device parameters to supply precise data to the simulator, minimizing device stress effects and maximizing power and reliability.
- **Logic Injection.** Locates repeated device patterns in the design and simplifies them to improve processing speed and performance.
- **Highest Verification Accuracy with Calibre DRC.** Pinpoints error detection with advanced device extraction and netlist comparison features, making Calibre DRC the best solution for verifying digital, analog, mixed-signal and SoC designs.
- **Tight Integration with Calibre xRC/xL.** Calibre xRC/xL directly reads LVS data structures and provides complete circuit netlist information integrated to the source schematic for back annotation.
- **Tight Integration with Calibre RVE.** Calibre LVS results and netlists can be viewed through the Calibre results viewing environment.
- **Seamless Design Flow Integration.** Calibre LVS can be invoked from within all popular layout environments through Calibre Interactive.

Capabilities of Calibre LVS

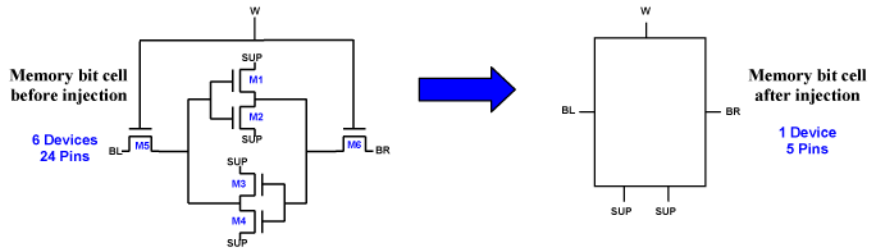
The industry-leading capabilities of Calibre LVS deliver exacting device layout and connectivity extraction as well as comprehensive circuit comparison and back annotation for verifying the actual IC layout with the schematic. The robust SVRF syntax language used in Calibre rule decks ensures that Calibre can accurately compare all device and circuit types. Calibre LVS has minimal text methodology dependencies to make ramp-up fast and easy.

Logic Injection

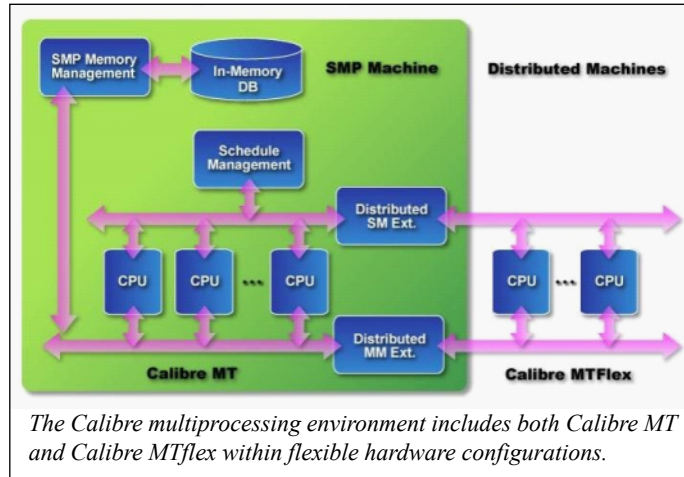
Calibre LVS uses an advanced logic injection technique to scan for repeated device patterns. When common, redundant patterns are found, the repeated devices are simplified and a level of hierarchy is injected that LVS uses during its comparison process. The types of logic that can be injected are memory bit cells, simple NAND NOR and INV gates, parallel/series gates and transmission gate multiplexers. The logic injection process greatly reduces the amount of system memory required by LVS, resulting in faster run times and superior overall performance. Another primary benefit of logic injection is that it can remain active in LVS and the user does not have to know any specifics about the design to be able to achieve better performance. Logic injection is 100% reliable, does not generate any false errors, and can be used with or without Hcells.

Accelerated Multi-Threading LVS Processing Power with Calibre MT and MTflex

Calibre MT and Calibre MTflex capitalize on pre-existing geometric threads generated by the Calibre hierarchical processing engine. The multi-threading CPU technology available with Calibre MT and the distributed network CPU processing capability of Calibre MTflex vastly increases the perform-



This memory bit cell example demonstrates the logic injection process for simplifying repeated structures.



The Calibre multiprocessing environment includes both Calibre MT and Calibre MTflex within flexible hardware configurations.

ance and speed of Calibre LVS. The reduction in processing time results in much quicker design completions.

Shorts Isolation

By identifying the shortest paths between mismatched text labels on the same electrical net, IC verification time can be sharply reduced by rapidly identifying and repairing the source of a short. Large power/ground shorts are graphically isolated by layer in Calibre's Results Viewing Environment (Calibre RVE).

Complete Device Parameter Analysis

Calibre LVS verifies that the physical layout of a device is equivalent to the device model by extracting and measuring its physical geometries in the

layout. Calibre LVS recognizes standard-named devices, then measures the device turns, wire space, core area, width and length until all physical parameters are analyzed. Next, LVS precisely compares these parameters to

the parameters in the models to ensure that what is being built is what was simulated. The following illustration demonstrates this comprehensive parameter comparison process.

Original Pcell
Read parameter method
If text = L1_abc
Then T = 1.5

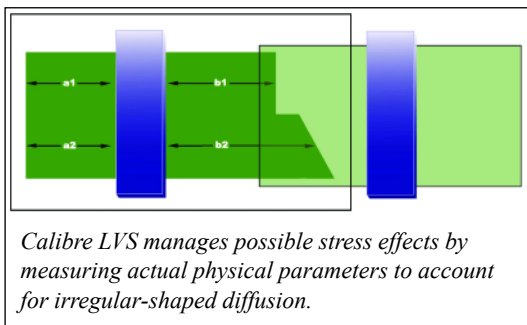
Modified Pcell
Physical Parameter Extraction
 $T = \text{NumCorners} * 90 / 360$
(Calibre method)

Case	Open-loop	Calibre
Original	T = 1.5	T = 1.5
Modified	T = 1.5	T = 1.75

The original pcell for inductor L1_abc has 1.5 turns. The modified pcell has been flattened and a short length of line was added to bring both terminals out on the same side of the inductor, effectively adding another 1/4 turn to the inductor, potentially increasing the actual inductance by up to 16%. A minor change to a crucial component can cause a significant shift in the desired performance of the design.

Managing Stress Effects

A parameterized cell can be placed during lower-level hierarchy cell creation. Later, at a higher level of the hierarchy, a layout designer may overlap the existing diffusion with new diffusion drawn at the parent cell. This design methodology saves space on the chip and determines the current flow and stress threshold of a device, but it can also create undesirable results that may go unnoticed during simulations. By measuring all the physical device parameters and supplying this precise data to the simulator, Calibre LVS maximizes device power and reliability while minimizing stress effects.



Calibre Design Flow Integration

Calibre can be invoked from within all popular design frameworks through Calibre Interactive. This gives designers access to an industry standard single-flow physical verification, LVS and parasitic extraction platform. Calibre is also integrated with place-and-route flows, so it can read LEF/DEF and annotated GDS data to take advantage of the connectivity information to produce gate-level netlists for gate-level simulators.

Calibre LVS with Calibre DRC

Combining Calibre LVS with Calibre's advanced Design Rule Checking (DRC) tool makes Calibre the best choice for verifying digital, analog, mixed-signal and SoC designs. Calibre DRC provides the fastest

methods possible to identify and repair design issues, including complex power-to-ground short circuits. The integrity of a design is thoroughly tested over a series of iterative invocations by running Calibre LVS along with Calibre DRC.

Calibre LVS with Calibre xRC/xL

For parasitic netlists to be useable in the designer's simulation testbench, the extracted layout netlist and parasitic devices need to be back-annotated to the schematic netlist. Consequently, a seamless interface between LVS and extraction is critical to ensure efficient data handling for both upstream design creation environments and downstream post-layout analysis. When Calibre LVS is used with Calibre xRC/xL, intentional device recognition (with device parameters) and parasitic device extraction at the transistor, gate and hierarchical levels are provided to achieve

the highest performance, capacity and yield from post-layout simulation and back-annotation of simulation results to the source schematic. Additional capabilities include:

- Standard and user-defined device extraction statements allow users to easily extract 3, 4, or N-terminal devices for digital, analog, and RF designs.
- Robust parameter extraction capabilities allow users to extract standard or complex equation-based user-defined parameters of any physical data.
- Rule writing is simplified through automated gate recognition, standard device reduction, and other options.
- Supported extraction and comparison of device M-parameters ensure tight tolerances for analog circuits.

- User-defined device reduction algorithms deliver unparalleled user control.
- Verilog translator provides easy input through a standard SPICE input.

Calibre LVS with Calibre Interactive

Identifying physical errors in an existing design database dramatically improves total debug time. After the errors are identified and debugged, a follow-up verification step is required. Calibre Interactive reduces the amount of time required to invoke these verification runs. Features include:

- Intuitive graphical interface.
- Interactive integration with popular layout tools automates the information required for verification.
- Pushbutton access from within the layout environment.
- Built-in memory for common run tasks with sunset support.
- Calibre LVS run options can be set on the fly.
- LSF (Load Sharing Facility) support reduces runtime environment constraints.

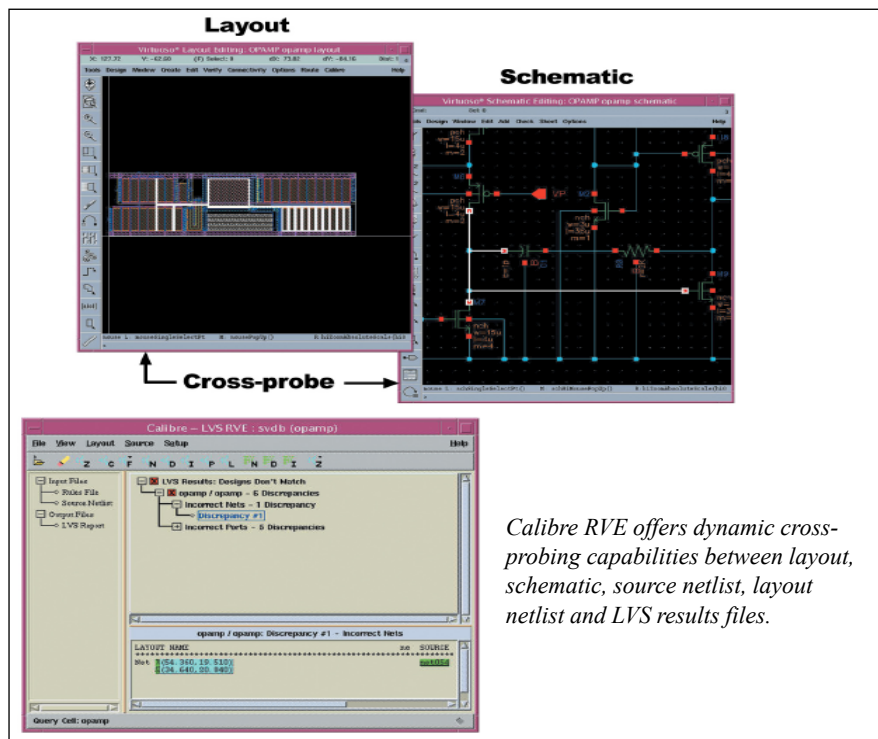
Calibre LVS with Calibre RVE

The time spent debugging a design can dramatically impact the total time to get it to manufacturing. Calibre RVE specifically address this problem by instantly identifying design errors in the user's own design environment.

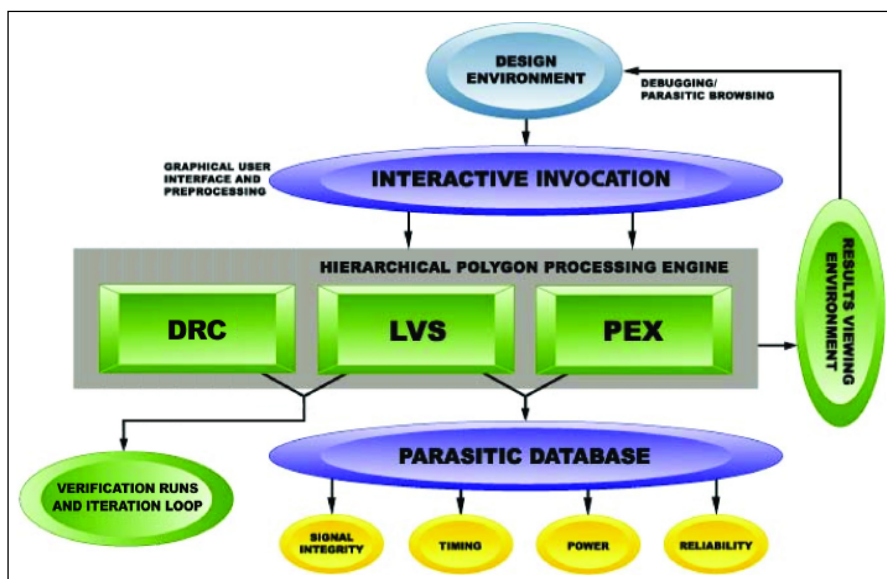
Calibre RVE highlights LVS results in the layout and schematic windows, as well as in the source and extracted netlists. This ability gives designers the ultimate graphical debugging tool for cell/block and full chip designs. Features include:

- User-friendly, intuitive graphical interface.
- Automated integration into common layout environments.

- Cross-probe results between layout, schematic, source netlist, layout netlist and Calibre LVS results files.
- Highlight to schematic capture products, including Mentor Graphics Design Architect-IC and Cadence Composer.
- Automated short isolation debugging makes even the most complex power or ground short easy to fix.
- Fast and intuitive hierarchical SPICE browser for source and layout netlists.



Calibre RVE offers dynamic cross-probing capabilities between layout, schematic, source netlist, layout netlist and LVS results files.



The Calibre design flow, showing the interactions and dependencies between Calibre Interactive, Calibre LVS, Calibre xRC, Calibre DRC and Calibre's results viewing environment.

For information, articles and papers, visit Mentor Graphics online at www.mentor.com

Copyright © 2005 Mentor Graphics Corporation. Mentor Graphics and Calibre are registered trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 SW Boeckman Road
Wilsonville, OR 97070-7777
Phone: 503-685-7000

Sales and Product Information
Phone: 800-547-3000
503-685-8000

Silicon Valley Headquarters
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Europe Headquarters
Mentor Graphics Corporation
Arnulfstrasse 201
80634 Munchen
Germany
Phone: 49 (0) 89 57096-0
Fax: 49 (0) 89 57096-400

Pacific Rim Headquarters
Mentor Graphics (Taiwan)
Room 1603, 16F
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-87252000
Fax: 886-2-27576027

Japan Headquarters
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3021



08/2005/IMG

1023980-w