

Parasitic inductance can greatly affect RF designs. Noise, distortion, impedance mismatch and jitter are natural phenomena that can cause a chip to fail if not accounted for in parasitic extraction. At higher frequencies, inductance can shift the frequency of oscillation in a VCO (as shown in the lower graphic example) and should be taken into account.

## Managing Inductive Effects in Nanometer Designs

With increasing operating frequencies, interconnect lines begin to exhibit inductive effects, which can have significant influence on chip behavior and performance. Parasitic on-chip inductance extraction is, therefore, crucial for accurate physical verification (simulation) and timely tape-out of high frequency RF, mixed signal and custom digital nanometer designs.

Calibre xL offers designers full-chip, fast and accurate extraction of frequency dependent loop inductance and loop resistance, and automatically accounts for return path change with frequency. Results of Calibre xL extraction highly correlate with field solvers and have silicon-tested accuracy.

## Key Product Benefits

- **Full-chip, high-performance, parasitic inductance extraction** provides highly correlated field solver and silicon-tested accuracy for analog, RF and custom digital nanometer designs.
- **Parasitic self-inductance extraction integrated with Calibre xRC parasitic RC extraction data** enables accurate analysis of high frequency effects in nanometer technology.
- **Accurate extraction of frequency dependent loop inductance and resistance** ensures optimized modeling of on-chip physical effects.
- **Efficient, realizable model order (RLC) reduction** provides manageable netlists and mixed-level outputs for ease of re-simulation without loss of accuracy.
- **Return-path selection and net-based extraction frequency selection** offers increased flexibility in performance and improved accuracy.
- **Seamless invocation, integration to Calibre LVS, xRC and RVE through Calibre Interactive** to enable cross-probing and debugging of results in popular layout environments.

## Calibre xL Inductance Solution

The difficulty in performing on-chip inductance modeling comes from the fact that inductive couplings are long range and that the return paths for the current are frequency dependent and not easy to determine or predict. Partial inductance approach, which does not require knowledge of the current return path, results in prohibitively large and dense inductance matrices for any reasonable size design, and produces netlists unmanageable for today's dynamic simulators.

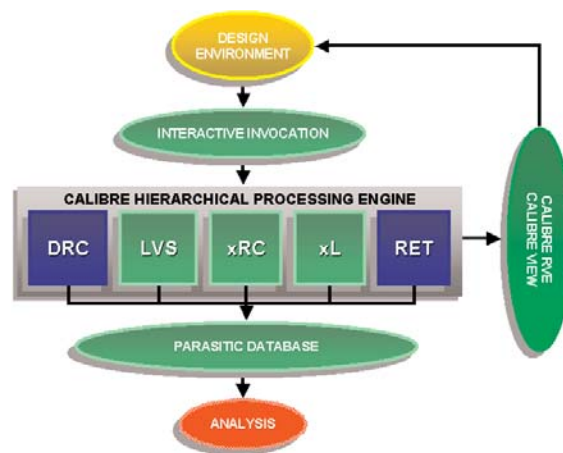
Calibre xL inductance calculation engine has unique, accurate and efficient way of calculating self loop inductances in complex designs. Built-in model order reduction reduces parasitics R,C, L data, and produces passive, realizable network for easy and efficient simulation, with no significant loss in accuracy. Built in filtering engine

eliminates inductively unimportant wires from accurate inductance extraction flow additionally improving simulation performance.

Calibre xL offers unprecedented flexibility through selected net extraction, automatic and user-defined selection of the return path, net-by-net base frequency selection and single run multiple frequency inductance extraction, with no need for calibration. Calibre xL has the performance to handle full chip extraction for micro-processor designs and the accuracy for analog/RF designs.

Calibre xL is fully integrated into the Calibre flow and with popular design environments. It offers designers inductance extraction independent of design style and flow. For analog/RF blocks, it offers necessary accuracy, and for digital designs, it also offers high capacity and performance.

Calibre xL extends the capability of Calibre xRC, the full-chip transistor-level parasitic extraction solution from Mentor Graphics. By reading Calibre LVS data structures directly, Calibre xRC/xL provides complete circuit netlist information integrated to the source schematic for back-annotation.



*Calibre xL is fully integrated with Calibre xRC and LVS, reading data structures directly for complete circuit netlist information and back-annotation.*

### Glossary of Inductance Terms Mentioned in this Datasheet

1. **Self loop inductance** is inductance associated with a signal and its current return path.
2. **Loop resistance** is a sum of resistances of a signal line and its current return path.
3. **Inductive coupling** manifests itself as a voltage induced in one net due to the current change in another net.
4. **Model order reduction** is a way to reduce the number of elements in your parasitic netlist.

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