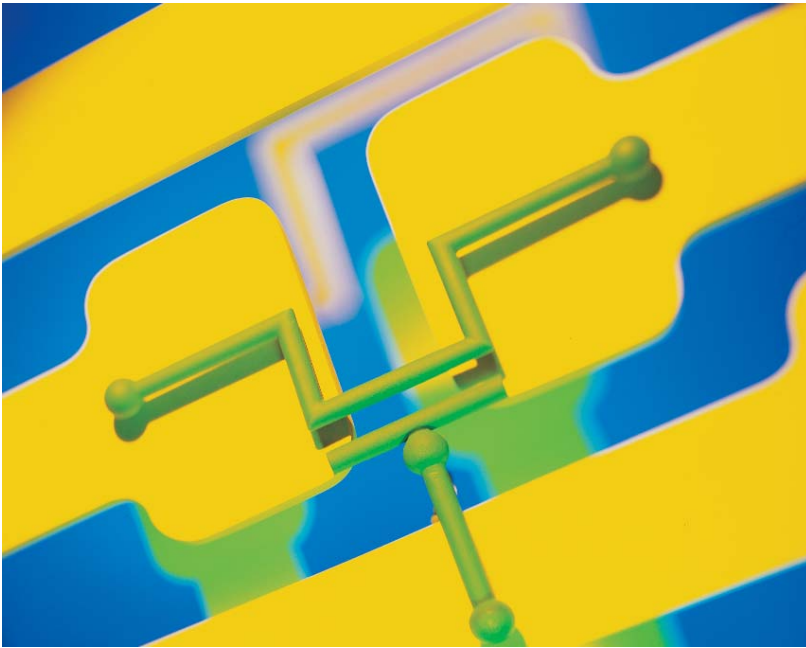


Calibre xRC-CB

Parasitic Extraction

D A T A S H E E T



Calibre xRC-CB is for designers requiring detailed parasitic extraction on cells, blocks and small chips. It is fully integrated with the Calibre product family as well as within popular layout and simulation environments.

Calibre® xRC-CB: Accurate, Transistor-Level Parasitic Extraction for Cells, Blocks and Small Chips

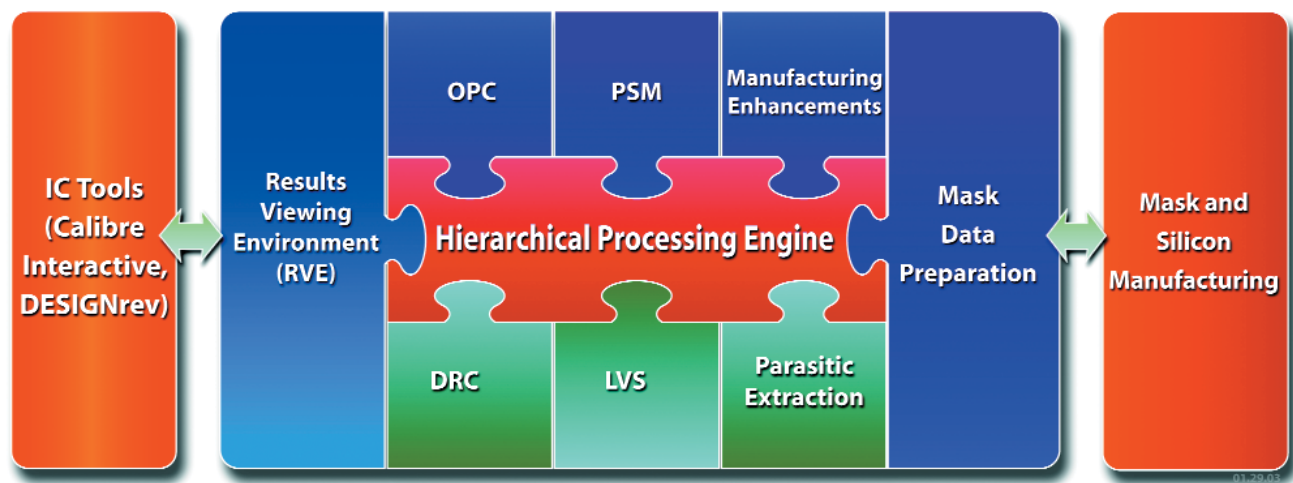
Designers developing small cells, blocks and chips require a parasitic extraction tool that delivers accurate parasitic data for comprehensive analysis and simulation.

Calibre xRC-CB parasitic extraction solution is independent of design style or flow, and is easily invoked from within popular layout environments via Calibre Interactive.™ Users can choose Lumped C, Distributed RC and Distributed RCC SPICE-type output formats to simulators such as Eldo, HSPICE and Spectre, regenerating output netlists in a different format without re-running the extraction engine, which saves time and effort. Calibre xRC-CB also integrates with Calibre View (extracted view) for post-layout simulation in the Cadence design environment.

When combined with Calibre LVS™, Calibre xRC-CB provides the only production-proven parasitic extraction tool set that ensures accurate back-annotation to the source schematic.

Key Product Benefits:

- Offers detailed and accurate transistor-level parasitic extraction for cells, block and small chips.
- Supports Lumped C, Distributed RC and Distributed RCC SPICE-type output formats for simulators such as Eldo, HSPICE and Spectre.
- Supports Calibre View (extracted view) to augment the Cadence DFII framework tools for post-layout simulation.
- Regenerates output netlist in a different format without having to re-run the extraction engine.
- Easily invoked from within Calibre Interactive.™ Results are accessed through Calibre RVE™, the robust results viewing environment.
- Fully integrated with all Calibre tools and is based on the robust Calibre hierarchical processing engine for optimum performance and capability.



The Calibre tool suite offers a complete design-to-silicon solution to ensure a confident design for manufacturing.

Calibre Offers a Complete Design-to-Silicon Solution

A powerful hierarchical engine is at the heart of the Calibre tool suite, which offers a complete IC and SoC design-to-manufacturing solution. Each tool is an excellent point tool on its own, but the combination of Calibre DRC™, Calibre LVS™ and Calibre RVE™ (results viewing environment) with Calibre xRC™, Calibre RET and Calibre MDP, simplifies and strengthens the design flow.

Calibre xRC parasitic extraction tool accurately models the parasitic effects of passive interconnects that can cause design failure in deep submicron IC designs. Automated interfacing of Calibre LVS to Calibre xRC provides simplicity (one rule file, one invocation) and automated back annotation for accurate parasitic extraction results, and ensures accurate and intentional device extraction with parameter calculation and parasitic device extraction for accurate simulation.

Calibre Interactive™ complements the Calibre physical verification tool suite by enabling designers to perform verification from within Cadence Virtuoso® and Mentor Graphics IC Station™ and Calibre DESIGNrev™. Together with Calibre RVE, Calibre Interactive provides a seamless, push-button interface, enabling designers to use a single platform for cell/block and full-chip physical verification.

The Calibre RET tool suite for Optical and Process Correction (OPC), Phase Shift Mask (PSM), Scatter Bars (SB) and Off-Axis Illumination (OAI) deliver silicon accuracy, fastest turn-around-time and excellent yield.

Calibre MDP allows for seamless continuation of the data manipulations required for RET techniques to the mask data format conversion in one batch run, keeping data hierarchically represented as long as possible.

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