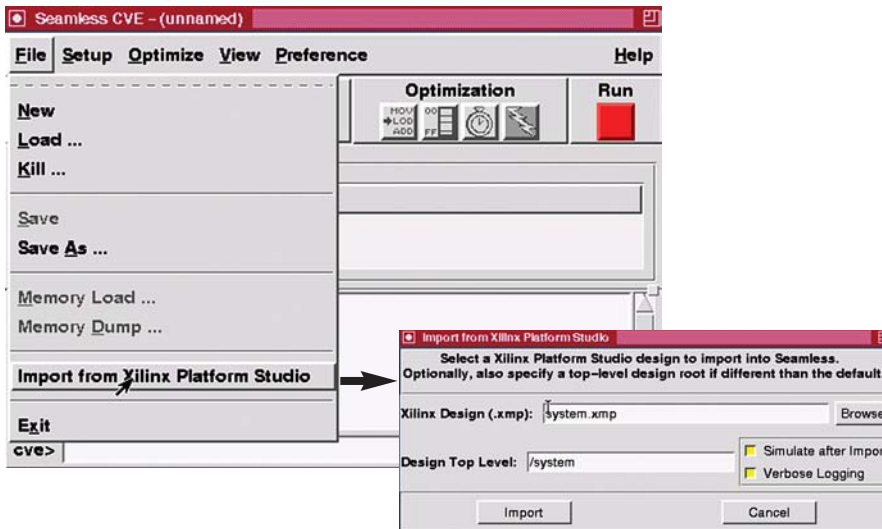


Seamless FPGA

Xilinx Virtex-II Pro and Virtex-4 Platform FPGAs with PowerPC 405



D A T A S H E E T



Seamless FPGA delivers high-performance, high validity co-verification for both Xilinx Virtex-II Pro platform FPGAs and the systems that utilize these leading-edge devices, reducing the risk of integration errors and improving time-to-market.

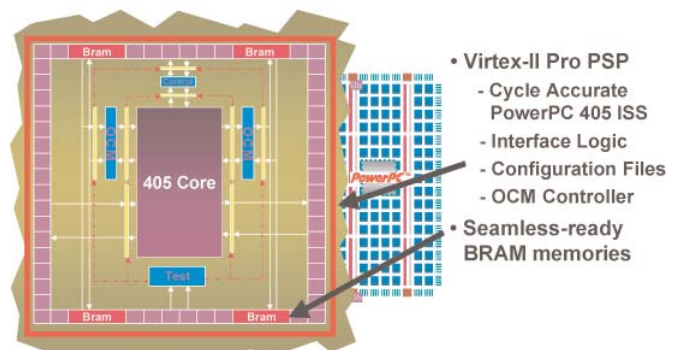
Key product features

- Cycle-accurate Seamless® PowerPC™ 405 PSP and Seamless FPGA
- Single button, automated Seamless FPGA set up from Xilinx XPS™
- Seamless FPGA-ready models for Virtex-II Pro on-chip memories
- Performance optimizations provide speed required to boot RTOS and run application code
- Full visibility and control of hardware and software execution
- Easy to use — no hardware or software changes required
- Windows®, Red Hat Linux®, and Sun Solaris™ platform support

Seamless FPGA

Mentor Graphics® and Xilinx have partnered to create a high-performance, high-accuracy co-verification solution for the Virtex-II Pro and Virtex-4 families of platform FPGAs. Starting with the industry-leading Seamless software and the cycle-accurate PowerPC 405 Seamless Processor Support Package (PSP), a solution tailored to the needs of engineers designing with Virtex-II Pro and Virtex-4 devices has been created.

Seamless FPGA enables the concurrent verification of hardware and software in both Virtex-II Pro and Virtex-4 devices and the systems that embed them. This verification takes place on a virtual prototype of the device or system and can be conducted weeks or months before a physical prototype is available. Using virtual prototypes provides levels of controllability, observability, and analysis that are often difficult to achieve with physical hardware.



Seamless FPGA provides out-of-the-box co-verification for embedded PowerPC cores.

Leading-Edge Price/Performance

The Virtex-II Pro and Virtex-4 families of Platform FPGAs provide the highest performance and lowest system cost with features integrated on one platform. This enables you to take advantage of hardware/software tradeoffs in a programmable environment.

PowerPC Embedded Processor Solution

The IBM PowerPC 405 core is an embedded processor core with a 32-bit Harvard architecture optimized for high performance, small die area, and low power.

Performance Optimization: The Key to Efficient Co-Verification

Seamless FPGA supports Dynamic Optimizations, a set of options which, under user control, routes memory requests from the ISS to the Coherent Memory Server, either directly, or via the logic simulator.

Utilizing optimizations allows the designer to switch between high-performance (direct access) and high-validity simulation as dictated by the system architecture and debug

requirements.

Seamless FPGA optimizations give you the ultimate in resolution, allowing the freedom to choose which areas of memory are optimized and when they are optimized — all without the need to halt or restart simulation.

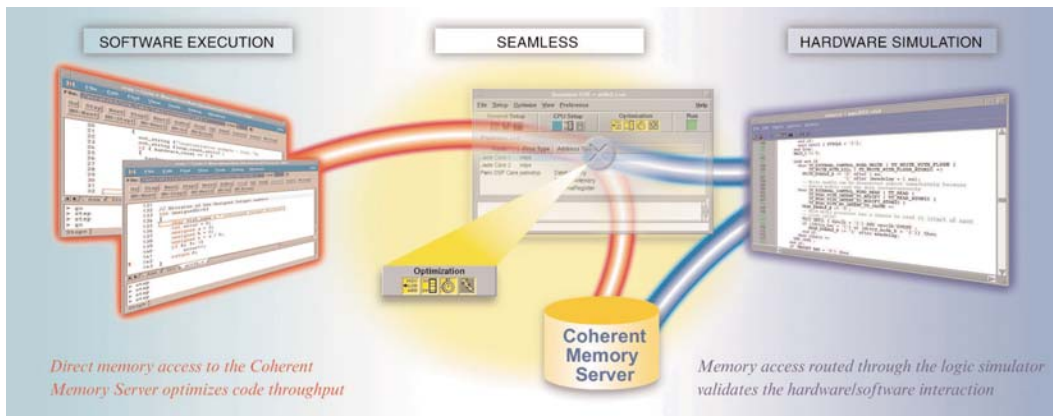
The Coherent Memory Server supports multi-processor designs and processors with multiple address spaces and a wide range of commonly used memory management techniques such as interleaving, remapping, error code correction, and parity checking.

Embedded Software Capability

Seamless FPGA is designed to simulate hardware/software interactions. Software functionality typically run on Seamless FPGA includes:

- Boot code
- Hardware diagnostics
- Device drivers
- RTOS

In addition, Seamless FPGA can run application code. There is no hard limit to the size of application, however simulation run-time becomes a practical limit for large applications.



The patented Seamless Coherent Memory Server empowers you to switch dynamically between detailed hardware verification and high-speed software execution.



Visit our web site at www.mentor.com/seamless for the latest product news.

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