

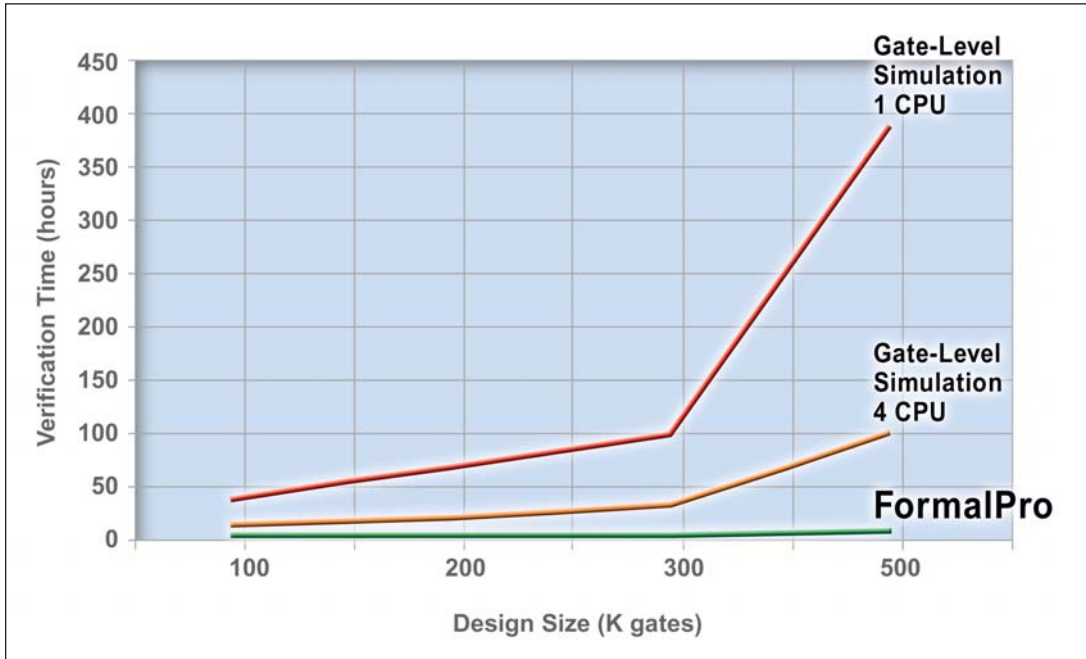
The FormalPro equivalence checker saves weeks in the verification of ASICs and ICs.

Major product features:

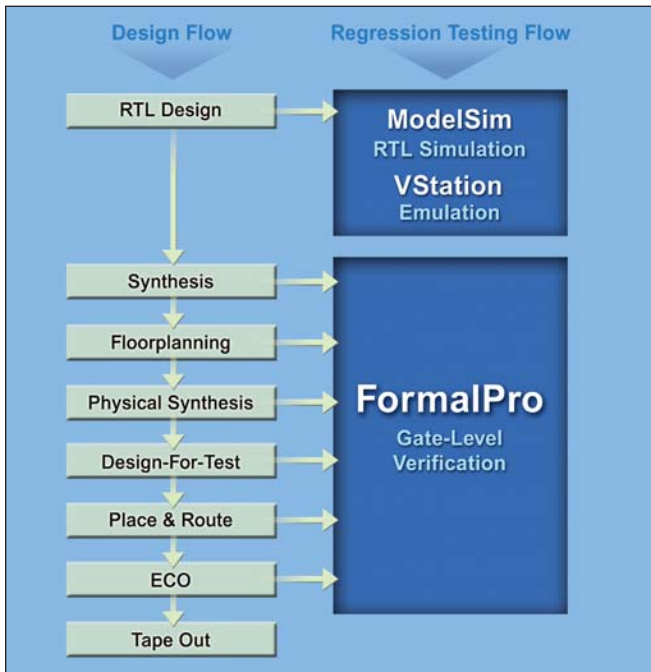
- 100 percent verification coverage without testbenches
- Full-chip verification of all designs from 100,000 gate ASICs to multimillion-gate SoCs
- Ultra high capacity ensures verification of physical flows for 130 nm and below without manual partitioning
- Distributed multiprocessor capability accelerates verification of the largest multimillion-gate designs
- Comprehensive debug tool identifies the exact location and cause of design errors
- Unique “what-if” capability investigates design modifications within the existing verification session
- Verification restart feature further reduces verification time by eliminating the need to recompile and rerun the entire verification with each incremental design and set up changes
- Intuitive graphical user interface guides user through all stages of verification set up

Complete Solution for Gate-Level Regression Testing of ASICs and ICs Larger than 100,000 Gates

FormalPro™ is the Mentor Graphics solution for gate-level regression testing of ASICs and ICs of 100,000 gates or more. FormalPro uses static verification techniques to prove that a design is functionally identical to its golden reference. This technique is orders of magnitude faster than traditional gate-level simulation. Designs that take days or even weeks to simulate with gate-level simulation can be verified in hours or even minutes using FormalPro. For designs greater than 100,000 gates, FormalPro is an essential verification tool in an ASIC design flow.



FormalPro performs gate-level regression testing orders of magnitude faster than gate-level simulation.



FormalPro works in conjunction with ModelSim® and VStation™ to form a scalable digital regression testing flow.

Gate-Level Regression Testing

Regression testing is the process of verifying that a design behaves as desired, and as previously validated, while it undergoes modification in the implementation phase. When in the RTL domain, this means re-simulating the design with hundreds or even thousands of pre-written tests to ensure that it still passes every time a modification is made. These simulations take many hours per test; however, this can be alleviated by running multiple simulations in parallel.

When the design goes to the implementation process — through logic synthesis and back-end physical implementation — regression testing at the gate-level requires a different methodology. The increase in volume of data from a few thousand lines of RTL code to hundreds of thousands of interconnected cells means that simulations can take days, weeks, or even months.

FormalPro is a regression testing tool that verifies that a design, after undergoing each of the implementation steps, is functionally identical to a previously signed off reference model. This methodology is orders of magnitude faster than simulation, ensuring that regression testing of designs at the gate-level can be performed in comparable if not faster runtimes than RTL regression tests.

100% Verification Coverage

Another advantage of FormalPro is that its static verification algorithms guarantee verification of 100 percent of the design, independent of testbenches. Unlike simulation, which tests nothing unless directed to by a testbench, FormalPro verifies every node in the design against the reference model (unless specifically directed not to). This ensures that even the subtlest introduced errors — for example, connectivity changes in the place-and-route process that alter functional behavior — are identified and reported.

Full Chip Verification

FormalPro's algorithms enable full-chip designs to be verified in their entirety. As designs pass through the physical implementation process, tools often optimize the design's hierarchy to meet timing-performance requirements. Therefore, an exact correspondence between lower-level blocks in a design is not possible. FormalPro's full chip methodology ensures that all designs, from 100,000 gates to beyond 20 million gates, can be verified in one process, without having to manually partition the design.

Furthermore, implementation of 130 nm designs and below creates new challenges for verification, and in particular, formal verification. Processes such as physical synthesis, floorplanning, layout, and clock tree synthesis have developed to improve timing closure. Many of these new techniques involve substantial manipulation of the design's hierarchy, to the point where the hierarchies in the logical and physical domains are drastically different. This has created a problem for verification

tools that rely on verifying designs hierarchically, or block-by-block, as there is no correspondence between the design hierarchies as the design moves through the implementation flow.

FormalPro's full-chip verification methodology ensures that designs can be verified regardless of whether physical design tools have optimized the design hierarchy.

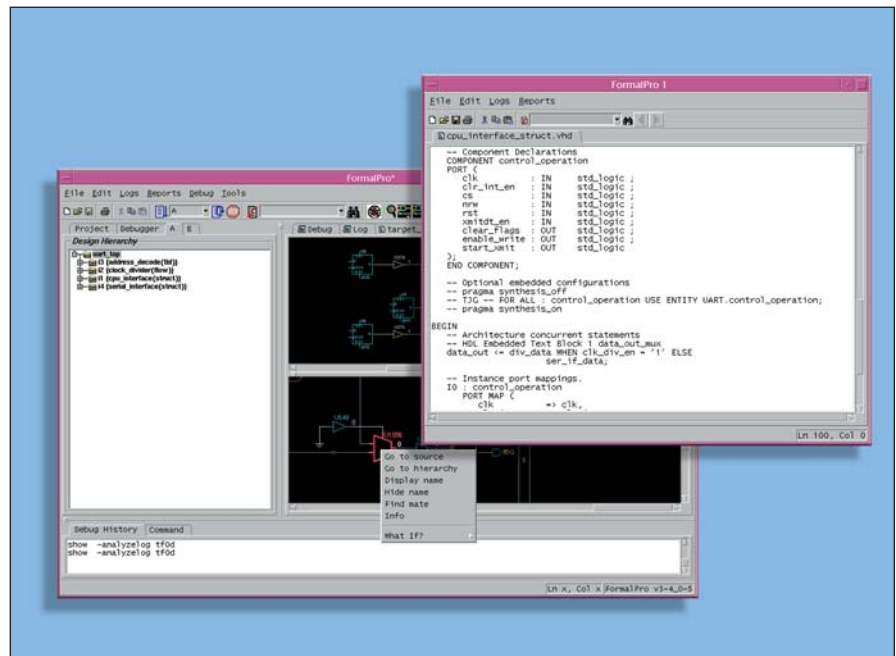
Debug Tool — The Shortest Route to a Correct Design

FormalPro's debugging capabilities dramatically reduce overall verification time by enabling engineers to identify and correct a faulty design hours or even days faster than other tools.

Unlike the verification process, the debug process requires human time, and is therefore more critical than machine runtime. It often takes much

longer to identify the location and cause of an error and then fix it, than it takes to run the tool, making debug one of the most important features of any verification tool.

FormalPro identifies the exact source of the functional error, not just the block or region in which the error manifests itself. FormalPro's hierarchical browser and schematic displays allow engineers to view the error within the context of either the hierarchical block or the whole design. It provides cross-probing between the schematics and the RTL or netlist source for intuitive debugging of design errors. And it displays the exact line of code corresponding to the error. In order to verify an error, FormalPro creates a difference vector that demonstrates the error in other verification environments, such as a simulator.



FormalPro's debug capabilities include cross-probing between schematics and RTL source code to trace design errors.

Unique What-If Capability Tests Design Modifications in Minutes

Once the cause of an error has been identified, FormalPro's unique what-if capability enables engineers to investigate design modifications within the existing verification session. When a functional difference has been reported, the user tests assumptions on how to resolve the problem using the what-if function. This capability saves hours, even days, in both debug time and the duration of iterations.

Verification Restart

FormalPro is the only static regression testing tool that provides a full verification restart capability. By allowing engineers to restart the tool at any stage in the verification process, FormalPro further reduces

verification time by ensuring that only the processing directly related to a design or set up change is rerun.

Furthermore, the verification restart capability enables engineers to start the debugging process on an identified error in parallel with a verification run, further improving productivity. Hence, for large designs, errors can be debugged and corrected as soon as they are confirmed, even while the full verification run has yet to be completed.

Finally, the verification restart capability enables efficient use of a company's computing resources. The computationally-intensive solving processes can be run on large servers, and, once this is completed, FormalPro can be restarted on an engineer's standard desktop computer for debugging the design.

FormalPro MP

FormalPro MP enables a farm of workstations or multiple CPUs to verify designs in parallel. FormalPro MP offers increased capacity and performance for the largest and most complex designs. It enables FormalPro to scale in both performance and capacity to handle multimillion-gate designs, typically encountered at 130 nm and smaller technologies. Formal Pro MP achieves this by distributing verification tasks across the available CPUs, providing scalable runtime and faster verification results.

Standard Language Support

FormalPro supports standard languages including VHDL-87 and 93, Verilog-95, and Verilog-2001.

Platform Support

FormalPro is supported on Sun Solaris™, Hewlett-Packard® HP-PA/UX, and Linux® based workstations.

Visit our web site at www.mentor.com/formalpro for more information, articles, or white papers.

Copyright © 2004 Mentor Graphics Corporation.

FormalPro and VStation are trademarks and Mentor Graphics and ModelSim are registered trademarks of Mentor Graphics Corporation. All other trademarks mentioned in this document are trademarks of their respective owners.

Corporate Headquarters
Mentor Graphics Corporation
8005 S.W. Boeckman Road
Wilsonville, Oregon 97070 USA
Phone: 503-685-7000
North American Support Center
Phone: 800-547-4303
Fax: 800-684-1795

Silicon Valley
Mentor Graphics Corporation
1001 Ridder Park Drive
San Jose, California 95131 USA
Phone: 408-436-1500
Fax: 408-436-1501

Europe
Mentor Graphics
Deutschland GmbH
Arnulfstrasse 201
80634 Munich
Germany
Phone: +49.89.57096.0
Fax: +49.89.57096.400

Pacific Rim
Mentor Graphics Taiwan
Room 1603, 16F,
International Trade Building
No. 333, Section 1, Keelung Road
Taipei, Taiwan, ROC
Phone: 886-2-27576020
Fax: 886-2-27576027

Japan
Mentor Graphics Japan Co., Ltd.
Gotenyama Hills
7-35, Kita-Shinagawa 4-chome
Shinagawa-Ku, Tokyo 140
Japan
Phone: 81-3-5488-3030
Fax: 81-3-5488-3031

